METHOD OF MANUFACTURING LATERAL DOUBLE-DIFFUSED METAL OXIDE SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

The present invention relates to a manufacturing method of an LDMOS transistor in which an ion-implantation process can be omitted.

A lateral double-diffused metal oxide semiconductor (LDMOS) is known as a small-sized power device having a small power consumption, and a structure and manufacturing method of the semiconductor are disclosed, for example, in Japanese Patent Application Laid-Open No. 1998-335663. In general, there are N-type and P-type LDMOSs. Here, a manufacturing method of a conventional LDMOS will be described hereinafter in terms of an example of the N-type.

Respective techniques such as oxidation, photolithography, and impurity implantation are used to implant N-type impurities such as phosphorus (P) into a predetermined region on a P-type semiconductor substrate. Subsequently, a diffusion technique is used to form an N-type well as a drain. Subsequently, techniques such as photolithography and ion-implantation are used to implant P-type impurities such as boron (B) forming a D well of the LDMOS into the N-type well, then the same resist is used to implant the N-type impurities such as arsenic (As), and the diffusion technique is used to form a P-type diffusion layer forming the D well and an N-type diffusion layer forming a

source. Here, since boron (B) is a small element and has a large diffusion coefficient as compared with arsenic (As), the P-type diffusion layer is formed to be deeper than the N-type diffusion layer.

Subsequently, a LOCOS forming technique is used to form a field oxide film for isolating elements from one another, an oxidation technique is used to form a gate oxide film on an inner surface of the field oxide film, and respective techniques such as known CVD, photolithography, and etching are used to form a polysilicon electrode in a channel forming region on the gate oxide film so that the electrode extends over the N-type well, P-type diffusion layer forming the D well, and N-type diffusion layer.

Subsequently, the photolithography technique is used to perform a desired patterning, and the resist and gate electrode are used as masks to implant the N-type impurities such as phosphorus (P) into the surface in the N-type well. Moreover, the diffusion technique is used to form the N-type diffusion layer forming a reduced surface drain (RSD) in the N-type well on a region having no P-type diffusion layer forming the D well.

Subsequently, the photolithography and implantation techniques are used to implant the N-type impurities such as arsenic (As) in a region as a part of the N-type diffusion layer from which electrodes of a drain and source are extracted, and implant the P-type impurities such as boron (B) in a region from which the electrode of the D well is

extracted. Furthermore, the diffusion technique is used to form the N-type and P-type diffusion layers, and finally the LDMOS is formed through contact formation, and wiring formation.

For the LDMOS formed by the aforementioned conventional method, after the N-type diffusion layer forming the source is formed, the gate oxide film is formed. Therefore, the gate oxide film on the N-type diffusion layer forming the source is formed to be thicker than the gate oxide film on the D well by accelerated oxidation. In this manner, a stepped portion is formed in a boundary having a difference in thickness in the gate oxide film in this manner. Therefore, an electric field distribution in the gate oxide film is not uniform, and there is uncertainty in reliability of pressure resistance of the gate oxide film.

SUMMARY OF THE INVENTION

The present invention may solve the aforementioned prior-art problem and provide a highly reliable semiconductor device. In the device, an accelerated oxidation during formation of a gate oxide film could be suppressed. Further, a stepped portion of the gate oxide film on a D well may be reduced.

A method of manufacturing an LDMOS transistor of the present invention comprises providing a semiconductor substrate of a first conductivity type having a well region of a second conductivity type formed on a surface of the

substrate. Ions of the first conductivity type are implanted into a part of the well region with a predetermined energy. The substrate is subjected to a heat treatment so that the implanted ions are diffused to form a diffusion region of the first conductivity type on the surface of the substrate. Then, a gate oxide layer and a gate electrode are formed on the surface of the substrate. Finally, a drain region is formed on the surface of the substrate. The predetermined energy for the implantation is set so that an accelerated oxidation during a formation of the gate oxide layer is inhibited.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1(A) to 1(F) are transverse sectional front views showing a manufacturing process of an LDMOS transistor according to a first embodiment of the present invention.

Figs. 2(A) to 2(D) are transverse sectional front views showing the manufacturing process of the LDMOS transistor according to a second embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figs. 1(A) to 1(F) are diagrams showing a manufacturing method of a semiconductor device according to a first embodiment of the present invention. A first diffusion layer (well) 103 of a second conductivity type is formed on a portion of a semiconductor substrate 101 of a first

conductivity type. A field oxide film 102 for isolating elements from one another can be formed using a known LOCOS forming technique, and a method similar to the conventional method can be used in a process for forming the first diffusion layer 103 of the second conductivity type. (Fig. 1(A)).

Subsequently, a first insulating film 104 is formed on the semiconductor substrate 101 of the first conductivity type, and a portion on the first diffusion layer 103 of the second conductivity type is opened (first opening). The first insulating film 104 is formed in a thickness of about 5000 angstroms by a known oxidation technique. Subsequently, a known photolithography/etching technique is used to open the first insulating film 104 in a region forming a D well, and a first insulating film 104b is formed in about 200 angstroms by the known oxidation technique.

Subsequently, a second diffusion layer (D well) 105 of the first conductivity type is formed in a portion in the first diffusion layer 103 of the second conductivity type via the first opening. The second diffusion layer 105 of the first conductivity type forming the D well is formed by implanting P-type impurities such as boron (B) by a known ion-implantation technique, and subsequently performing a heat treatment in an N_2 gas atmosphere at 1000°C for about 20 minutes by a known diffusion technique. (Fig. 1(B)).

Subsequently, an impurity 106 of the second conductivity type set to be introduced inwards via a main

surface of the second diffusion layer 105 of the first conductivity type is introduced into the second diffusion layer 105 of the first conductivity type via the first opening (source). A known high-energy ion-implantation technique can be used in forming a source region, and the N-type impurity 106 such as arsenic (As) is implanted with an energy amount of 500 keV, and a dosage of about $5.0 \times 10^{15}/cm^2$. In this case, for an arsenic ion, a high-energy ion-implantation is set so that a stepped portion of an oxide film is not formed on the D well by the subsequent heat treatment during formation of a gate oxide film and the arsenic ion is diffused to the surface by the heat treatment. (Fig. 1(C)).

Subsequently, the first insulating film 104 is removed, a second insulating film (gate oxide film) 107 is formed on the semiconductor substrate 101 of the first conductivity type, and the impurity 106 of the second conductivity type is activated to form a third diffusion layer 108 of the second conductivity type. After the first insulating films 104, 104b are removed, the second insulating film 107 is formed in about 300 angstroms using the known oxidation technique. In this case, the impurity 106 of the second conductivity type introduced into the region forming the source is diffused to the surface, and the third diffusion layer 108 of the second conductivity type is formed (Fig. 1(D)).

Subsequently, a gate electrode material is formed on

the second insulating film 107, and a gate electrode 109 of LDMOS is formed and extended from a partial region of the third diffusion layer 108 of the second conductivity type at least onto the region of the second diffusion layer 105 of the first conductivity type excluding the third diffusion layer 108 of the second conductivity type. For the gate electrode 109, for example, polysilicon is formed in a region forming a channel using the known CVD/photolithography/etching technique. A fourth diffusion layer (RSD) 110 of the second conductivity type is formed in a region excluding the second diffusion layer 105 of the first conductivity type in the first diffusion layer 103 of the second conductivity type. (Fig. 1(E)).

Subsequently, a fifth diffusion layer 111 of the second conductivity type is formed in a region on a side opposite to that of the second diffusion layer 105 of the first conductivity type via the fourth diffusion layer 110 of the second conductivity type in the first diffusion layer 103 of the second conductivity type. Additionally, a sixth diffusion layer 112 of the second conductivity type is formed in a portion in the third diffusion layer 108 of the second conductivity type.

Subsequently, the known photolithography technique is used to perform a desired patterning, and a resist and the gate electrode 109 are used as masks to implant N-type impurities such as phosphorus (P) into the surface in the first diffusion layer 103. The fourth diffusion layer 110 of

the second conductivity type forming an RSD is formed by the known diffusion technique.

Subsequently, a seventh diffusion layer 113 of the first conductivity type is formed in a portion in the second diffusion layer 105 of the first conductivity type and connected to the second diffusion layer 105 of the first conductivity type. The known photolithography and implantation techniques are used to implant the N-type impurities such as arsenic (As) in a region from which electrodes of the drain and source are extracted with an energy amount of 60 keV, and a dosage of about $1.0 \times 10^{15}/cm^2$. The P-type impurities such as boron (B) are implanted in a region from which an electrode of the D well is extracted with an energy amount of 30 keV, and a dosage of about $1.0 \times 10^{15}/cm^2$. (Fig. 1(F)).

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Finally, the known diffusion technique is used to form the fifth, sixth, and seventh diffusion layers 111, 112, 113. Finally, after a contact and wiring are formed, the LDMOS is formed. Additionally, a known technique is used in forming the contact and wiring (not shown).

A known semiconductor manufacturing technique can be used in respective processes such as photolithography, etching, deposition of various members, implantation, diffusion, contact formation, and wiring formation. This also applies to the following second embodiment of the present invention.

According to the first embodiment of the present

invention, when the impurity of the second conductivity type forming the source region is implanted by high-energy ion-implantation, accelerated oxidation during formation of the gate oxide film can be suppressed, the stepped portion of the gate oxide film on the D well is reduced, and a highly-reliable semiconductor device can be provided.

Figs. 2(A) to 2(D) are process sectional views showing a second embodiment of the present invention. First, a first diffusion layer (well) 203 of the second conductivity type is formed in a portion on a semiconductor substrate 201 of the first conductivity type. Next, a first insulating film 204 is formed on the semiconductor substrate 201 of the first conductivity type. A portion on the first diffusion layer 203 of the second conductivity type is opened, and a first opening 204a is formed. (Fig. 2(A)). A second diffusion layer (D well) 205 of the first conductivity type is formed in a portion in the first diffusion layer 203 of the second conductivity type via the first opening 204a. (Fig. 2(A)).

Subsequently, by the known photolithography and etching techniques, a resist 213 is formed, and in the first insulating film 204, an opening 213a is formed as a region from which the drain electrode and source electrode of the LDMOS are extracted in a part of a region in which the second diffusion layer 205 of the first conductivity type is not formed in the first diffusion layer 203 of the second conductivity type. The resist 213 is removed, and an

impurity 206 of the second conductivity type set to be introduced inwards from a main surface of the semiconductor substrate 201 of the first conductivity type and the second diffusion layer 205 of the first conductivity type simultaneously via the second and first openings, so that the source and drain are formed. (Fig. 2(B)).

Here, by the known high-energy ion-implantation technique, the N-type impurities such as arsenic (As) are implanted with an energy amount of 500 keV, and a dosage of about $5.0 \times 10^{15}/cm^2$. In this case, for the implanted arsenic ion, the high-energy ion-implantation is set so that the stepped portion of the oxide film on the D well is not formed by the subsequent heat treatment during formation of a gate oxide film 207, and the arsenic ion is diffused to the surface by the heat treatment. (Fig. 2(C)).

Subsequently, the first insulating film 204 is removed, the second insulating film (gate oxide film) 207 is formed on the semiconductor substrate 201 of the first conductivity type, and the impurity 206 of the second conductivity type is activated to form a third diffusion layer 208 of the second conductivity type.

Subsequently, the gate electrode material is formed on the second insulating film 207, and a gate electrode 209 of LDMOS is formed and extended from a partial region of the third diffusion layer 208 of the second conductivity type at least onto the region of the second diffusion layer 205 of the first conductivity type excluding the third diffusion

layer 208 of the second conductivity type. Subsequently, a fourth diffusion layer (RSD) 210 of the second conductivity type is formed in a region excluding the second diffusion layer 205 of the first conductivity type in the first diffusion layer 203 of the second conductivity type.

Subsequently, a sixth diffusion layer 212 of the first conductivity type is formed in a portion in the second diffusion layer 205 of the first conductivity type and connected to the second diffusion layer 205 of the first conductivity type. (Fig. 2(D)).

The second embodiment is similar to the first embodiment in and after a process of removing the first insulating film 204 and forming the second insulating film (gate oxide film) 207.

According to the second embodiment of the present invention, in addition to an effect of the first embodiment, there is an effect that the introduction of the impurity of the second conductivity type for forming the source region and the introduction of the impurity of the second conductivity type for extracting the drain and source electrodes are simultaneously performed, and an ion-implantation process can therefore be reduced.

The preferred embodiments of the manufacturing method of the LDMOS transistor according to the present invention have been described above with reference to the accompanying drawings, but the present invention is not limited to these embodiments. A person skilled in the art

would apparently develop various modifications within a category of technical thoughts defined by the appended claims, and such modifications are also deemed to be naturally within the technical scope of the present invention.

As described above, according to the present invention, there can be provided a highly reliable LDMOS transistor in which accelerated oxidation during formation of the gate oxide film can be suppressed and therefore the stepped portion of the gate oxide film on the D well is reduced.